* Shammah Thao  
  • [shammah1230gmail.com](mailto:resume@pragmaticengineer.com) • (916)667-5376 • [Github.com](https://github.com/sthao0) •[linkedin](http://www.linkedin.com/in/shammah-thao)

## EDUCATION

**California State University, Sacramento 2016 - Expected 2022**

* BsCPE Computer Engineer

## TECHNOLOGIES AND LANGUAGES

* Languages: Java, Verilog, Vhdl, C/C++
* Software: Multisim, Vivado, Wireshark, Putty, initial state
* Skills: Circuit Analysis and Construction, Computer Assembly

## PROJECTS

* **Weather Station Project** *(Computer Interfacing)*
  + Designed and completed a working weather station that can sense wind speed, temperature, wind direction, as well as barometric pressure. This is all actively updated through a finite state machine implemented within the code. Using the on- board sensors of the attached sense hat, I was able to create a finite state machine that is able to display weather data in real time. The whole project was done in python to help further aid understanding of the language.
* **PCI Arbiter (***Computer Hardware Design)*
  + Created and implemented a fully functioning PCI Arbiter using Verilog with the methodologies learned in class. The purpose of this project was to understand at an intimate level hot the PCI Arbiter grants permissions to allow for multiple masters to be able to write to the data bus using the round robin scheme.
* **Simplified Microprocessor Design** *(Advanced Logic Design)*
  + Designed a simplified microprocessor using the block diagrams provided in the lab manual. Used the given structural hierarchical design method to implement within each individual sub design using Verilog. Created a test bench simulation of the top-level microprocessor data path design.
* **State Machine Project** *(Intro to Logic Design)*
  + Designed an “implied” system clock state machine solution in accordance to a diagram provided by the professor. Utilized K-maps to find equations for each of the inputs to the D flip-flops. Used D flip-flops and assign statements to implement the design. Used the design to create a Verilog code that is able to be assigned pins to test each part of the state machine for correct outputs.

## WORK EXPERIENCE

Waitstaff, Carlton Senior Living Oct 2017 – Feb 2020

Sacramento, CA

* Worked in a team orientated, fast-paced environment, providing exceptional customer service to hundreds of clients
* Mentored 4 trainees – applying personal experience giving useful insights resulting in a well prepare team